EE/CprE/Se 492 Weekly Report 3
2/14/25 - 2/27/25
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps and Project Lead
John – Testing Lead
Nicholas – Harden and Verification lead
Levi – Communication Interfaces Lead

Weekly Summary

These past two weeks we have been able to get a good basis to our CyGRA, we were able to perform a MAC operation in 2 cycles and simply utilizing the memory that was in the CyGRA. Additionally we have started to get some testing setup on an FPGA to ensure our components work both in simulation and hardware.

Pask Week Accomplishments

- Calvin:
    - Worked on getting the caravel project running on the FPGA with Camden and John
    - Made a memory interface bus priority splitter for when we need a second memory interface when we implement the DMA into the CyGRA
    - Finished the CyGRA v1.0
- Camden:
    - Started to try and get the caravel on the FPGA to enable testing
    - Found repository that is supported by efabless that enables this, but was unable to get it to generate the bitstream, some errors that need to be fixed or reviewed
- John:
    - I was able to work on updating the previous version of the CyGRA, created a decoder and processing element array to split the functionality of the CyGRA into its own modules for ease of use.
    - Was able to create some simple test benches to test the decoder and was able to perform a MAC operation using our CyGRA

    - Working with Nick we were able to generate a bitstream with SPI I/O to communicate with the PMOD and off-chip memory
- Levi:
    - Last update (missed last report) worked on selecting base IP for SPI Master unit and commenting out code and implementing testbench on said IP, did not get to implementing interactions with the memory controller
    - Current update: Worked on getting benchmarks from embench to run on the picorv32 processor implemented on the Zynq FPGAs via Vitis in 2041 Coover.
- Nicholas:
    - Integrated the Pico, Memory Controoler, WBS, cache, and memory into a caravel wrapper for RTL testing
    - Worked on a Vivado project containing non-CyGRA components

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	• CyGRA v1.0 • Memory splitter • Moral Support	10	100.044
Camden	• Found efabless repo for testing on fpga • Started working on project in vivado and following the provided documentation • Helped generate bitstream for separate FPGA testing outside of caravel	8	80

John	• CyGRA v1.1
	  ○ Decoder
	  ○ PE Array
	• Generated bitstream to communicate with off chip memory
		12	100

Levi	• Last update: SPI master unit	Last: 8 Current: 6	82

	• Current update: embench testing on FPGA of picorv32 processor as a baseline		
Nicholas	• Integrated design into Caravel Wrapper • Wrote tests for design • Working on getting CyGRA-less design working on an FPGA to perform benchmarks	10	106

Plans for Upcoming Week

- Calvin:
    - Finish the CyDMA v1.0
    - Get it incorporated into the fpga testing flow
- Camden:
    - Continue trying to get the FPGA testing to work based on the efabless documentation and repo
    - Look into the tooling that Gregory ling created that is supposed to create a vivado project with caravel (wasn't able to get to work so far)
- John:
    - Work on updating the CyGRA based on our benchmarks
    - Work on being able to load off-chip memory
- Levi:
    - Work with Nicholas for system level testing between the SPI Master and memory controller
    - Scope out more benchmarks and run baseline tests on the FPGA picorv32 implementation and select metrics for comparison
- Nicholas:
    - Continue working on getting FPGA simulations of the base user project and the project inside the caravel wrapper working.
    - Create a unit to interface the SPI Master with the memory controller.

Summary of weekly advisor meeting

Professor Duwe was happy to see our progress, suggested that before we continue working on the CyGRA we find some benchmarks so that we know what accelerations we need to accelerate. We also need to learn how we are going to load off chip memory, he suggested using the memory PMOD that was developed by Chip Forge. He also suggested having a good portion of our project hardened so that we are able to speed up the final process with getting it onto the chip with the other projects.